

The Challenges for Semiconductor Design

The Maskmaker's Perspective

Taiwan + China Semiconductor Industry Outlook 2004



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Outline



- A mask company addressing design?!?!
- Fabless-Foundry trends
- Effects on, and of, Taiwan and China



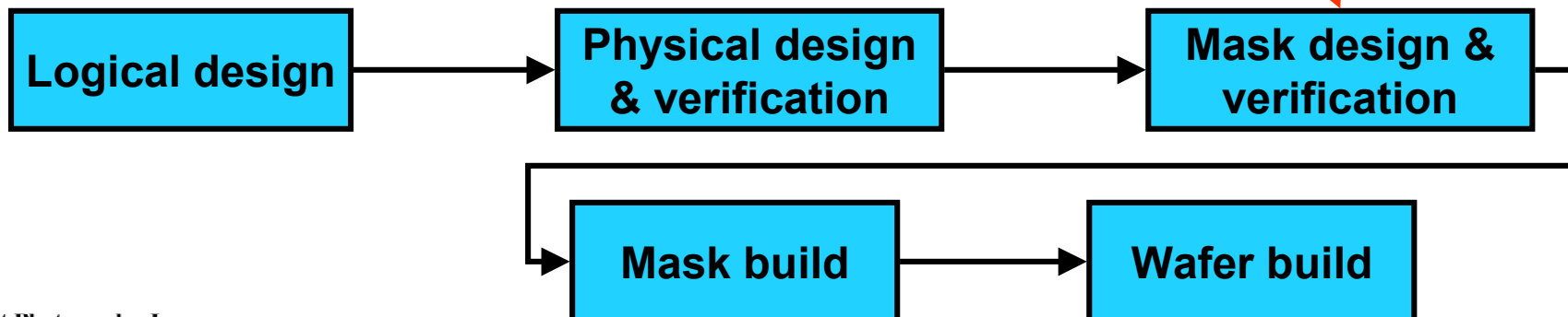
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A mask company addressing design?!?

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- The mask is the first point at which design data are reduced to a physical object (mask makers maintain design data “vaults”)
- Mask technology drives the performance, capability, and reliability of semiconductors
- Lithography/mask performance limitations cause design complexity (RETs, or Optical Proximity Correction and Phase Shifting Masks)
- The mask maker’s view of semiconductor manufacturing.



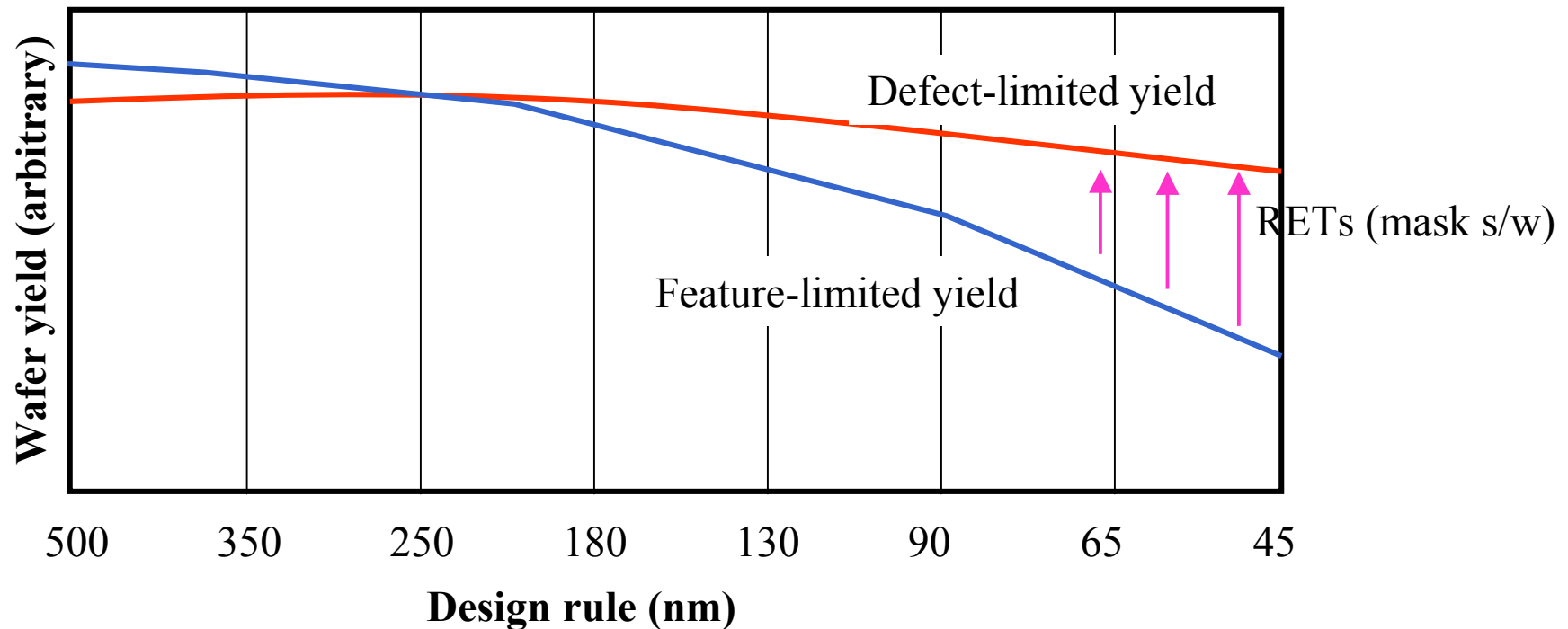
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What does mask design do for us?



- EDA s/w enables lithography solutions (RETs: OPC, PSM) that weren't required at large design rules



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Mask design evolution

- To maintain manufacturability and yields, mask complexity has increased

	0.25 μm	0.18 μm	0.13 μm	0.09 μm
Circuit design				
	DRC			
Mask design		Rules-based OPC	PSM, fill	Model-based OPC
	Tapeout			
Mask build	MDP			mOPC
Wafer build				



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Fabless/foundry trends I



Mask merchants were the original “front end” foundries ⇒ let’s learn from this

- Captive consolidation due to high mask manufacturing costs
- Centralized R&D ⇒ technology deployment for mfg near the customer
- Customers incorporate mask effects into IC design

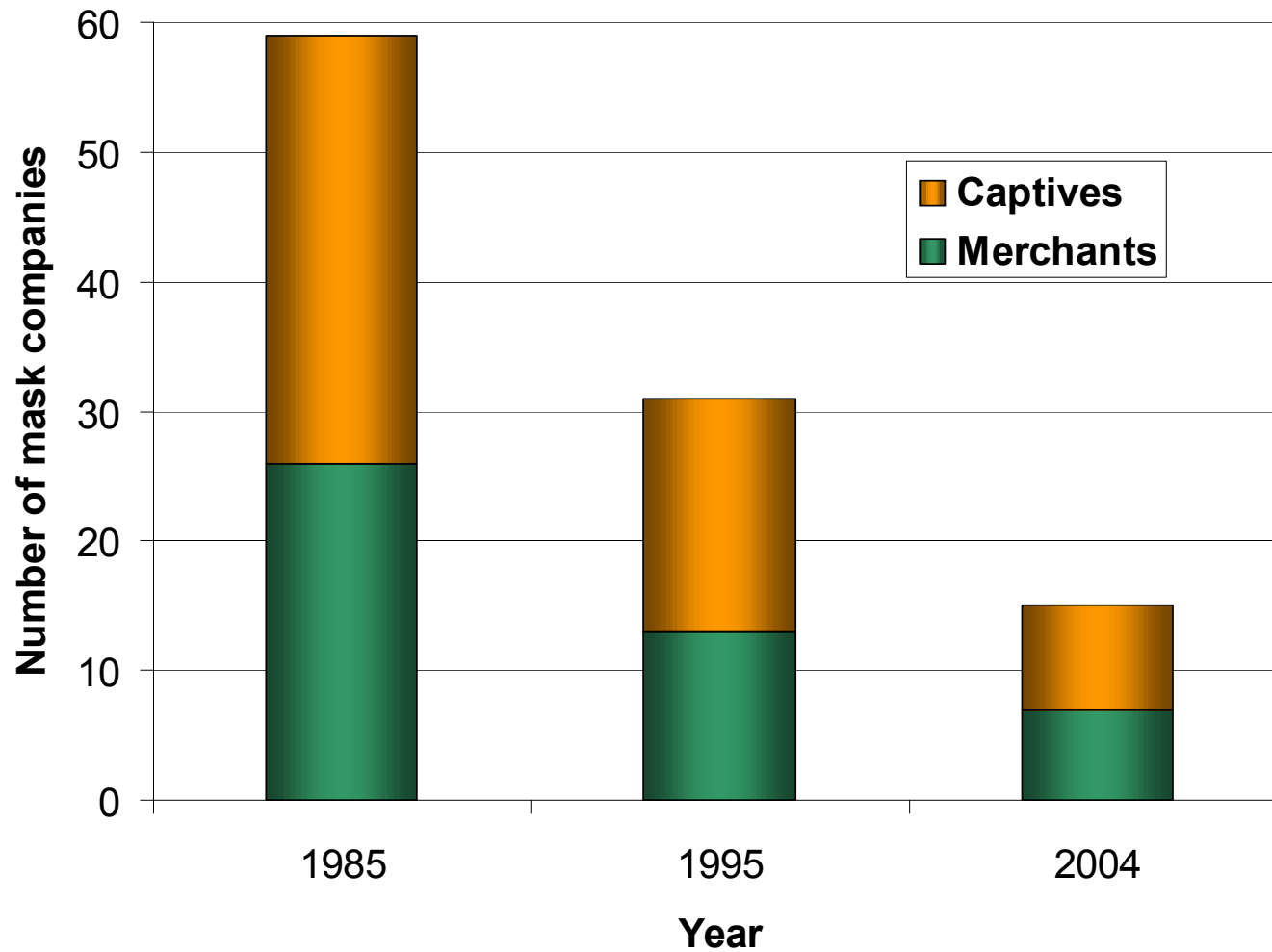


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Less Mask Companies Over Time

~50% decrease every 10 years



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Fabless/foundry trends II



IC foundry trends

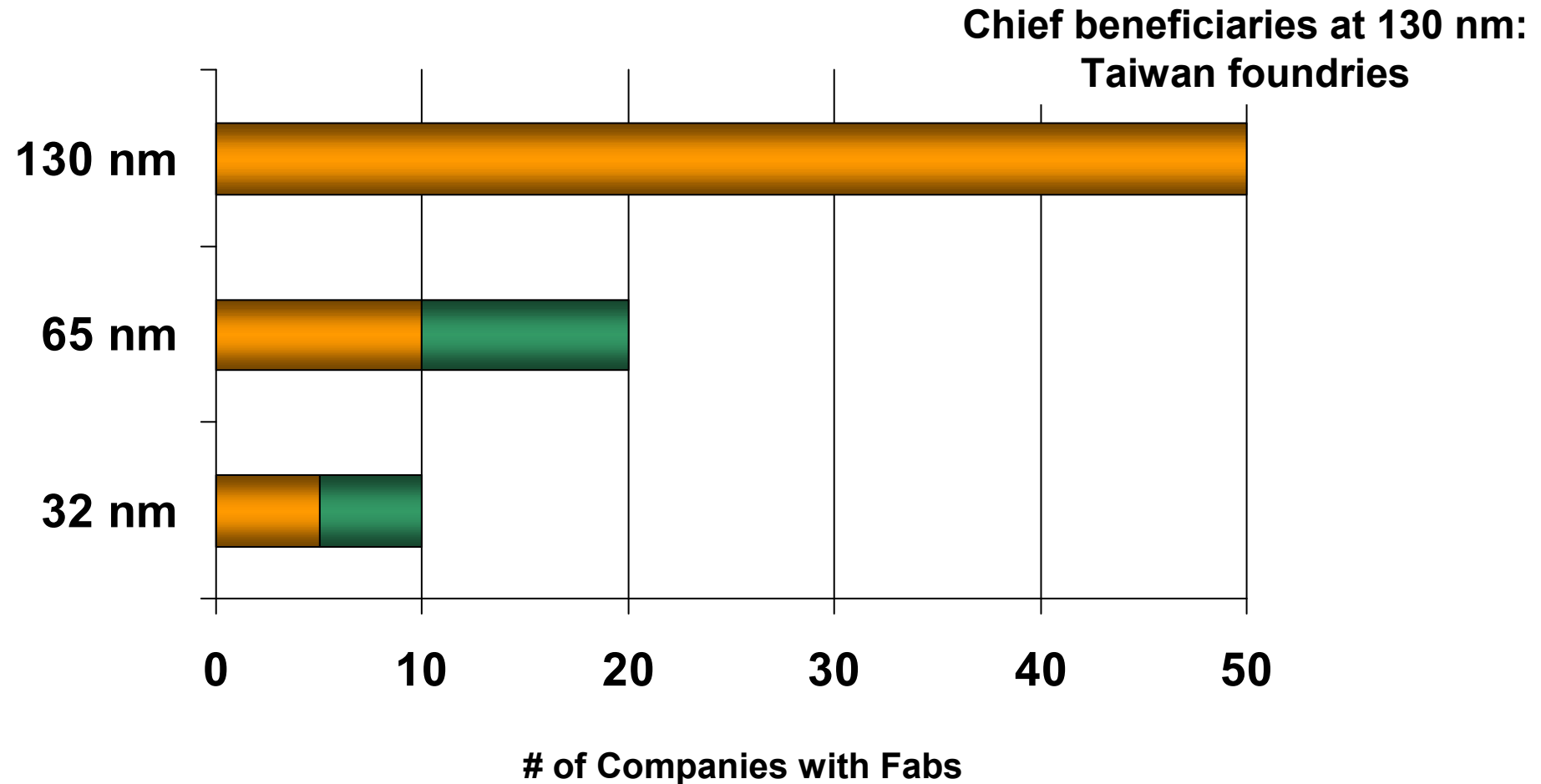
- IDMs offload excess production demands
Provide manufacturing technology to foundry partner(s)
- Fabless companies focus on design and distribution
- Customers incorporate foundry manufacturing rules into IC design
- Foundry may or may not have mask capability



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Companies building IC fabs at each node



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IC and mask foundry models

- Integrated IC-mask foundry model
 - Easy initial integration of mask into design process
 - No competition \Rightarrow more expensive masks

- Separate IC-mask foundry model
 - Requires conscious, tight communication between designer and both foundries
 - Competition \Rightarrow less expensive masks



Collaboration Models

Purpose	Companies	Location
IC process R&D cost sharing	ST Microelectronics, Freescale, Philips	France
Mask R&D & manufacturing	AMD, DuPont Photomasks, Infineon	Germany
Chip performance, yield, and manufacturability	Applied Materials, ARM, Artisan, Cadence, TSMC	Distributed



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The Taiwan and China markets



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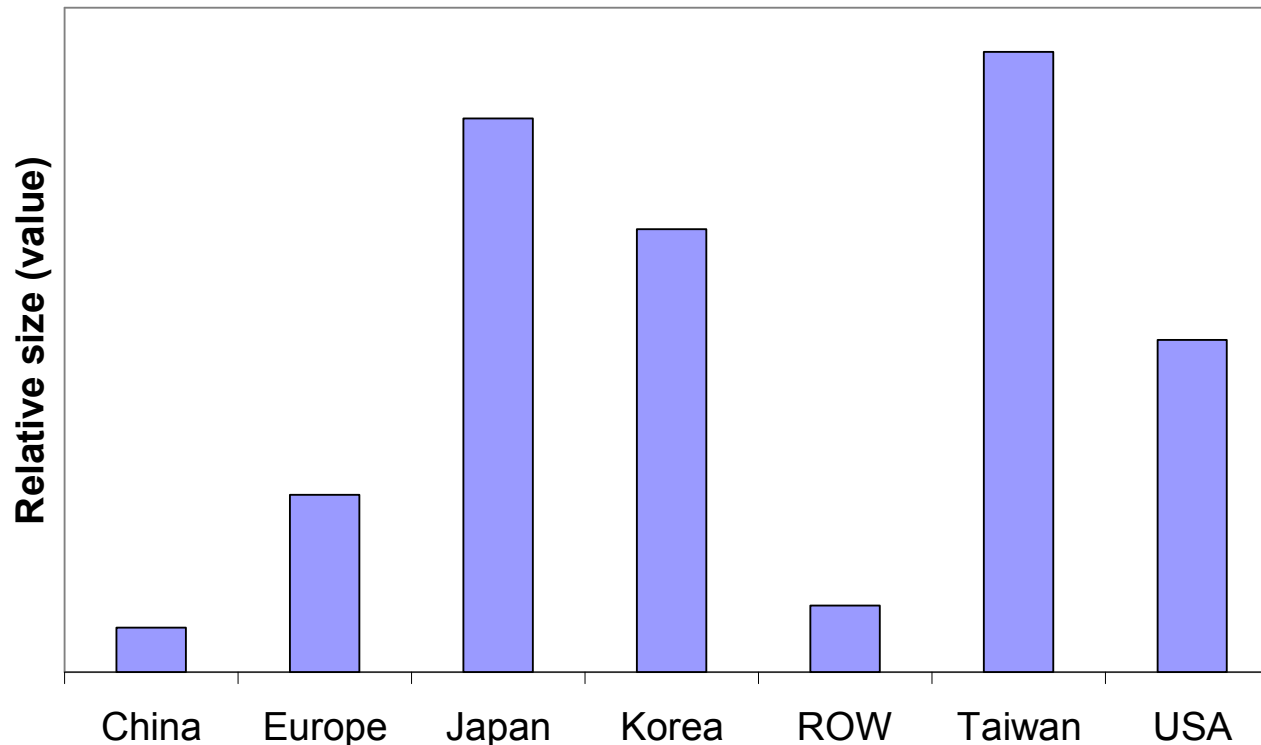
Taiwan

- IC demand \ll production capacity
⇒ IC exporter
- Full technology range
- Very large mask market
- Strong foundry investment

China

- IC demand \gg production capacity
⇒ IC importer
- Most technology $>$ 250 nm DR
- Mask market $<$ 5% of global total
- Strong foundry investment

Relative Sizes of Mask Markets



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Photomask technology in China



- Install mature manufacturing technology
- For most Chinese IC mfrs: 180/130 are next two nodes
 - Lithography strategy is already defined
 - Modest R&D investment is needed
 - Advantage: very fast time-to-market
- **DPI approach:** match market and technology requirements
 - **Local capacity**
 - **Local capability** } expand/improve to match market
 - **Regional support:** meet advanced technology requirements



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Summary



- Masks bridge semiconductor design and manufacturing
 - Mask design is a yield enabler at advanced nodes
 - The mask is an optical element in semiconductor lithography

- The semicon foundry trend is similar to the mask foundry trend
 - Consolidation into fewer producers
 - Supplier and customer focus on what each does best
 - Collaboration models are developing and maturing

- Taiwan and China have become the foci of the foundry trend
 - Different markets, different production capabilities
 - China market is just emerging, mainly at mature mfg nodes



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